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detecting when the chemical mechanical polishing process has removed the sacrificial layer.

REMARKS

In the Office Action mailed November 4, 2002 (Paper No. 11), the Examiner rejected Claims 30-32, 34, 37, 56-58, and 62 of the pending application as being unpatentable under 35 U.S.C. §103(a) over Han (US Patent Number 6,107,191) in view of Sandhu et al. (US Patent Number 5,069,002). The Examiner further rejected Claims 33, 35-36, and 59-61 of the pending application as being unpatentable under 35 U.S.C. §103(a) over Han (US Patent Number 6,107,191) in view of Sandhu et al. (US Patent Number 5,069,002), and further in view of Tobben et al. (US Patent Number 6,103,456).

In the Office Action, the Examiner rejected Claims 30, 56 of the pending application as being unpatentable under 35 U.S.C. §103(a) over Han (US Patent Number 6,107,191) in view of Sandhu et al. (US Patent Number 5,069,002). However, the Applicant notes that the Han reference fails to suggest using a CMP planar etch to remove the conductive and sacrificial layers until the shield layer is reached so as to ensure that the conductive and sacrificial layers have been removed following the CMP planar etch. Further, to the extent that the Han reference is removing conductive material from the upper dielectric layer using a planar etch, Han does not use the upper dielectric layer to inhibit thinning of the underlying dielectric layers during the planar etch in the manner claimed by the Applicant.

In particular, Han teaches etching excess conductive material without concern for thinning underlying layers. Even though the Sandhu et al. reference suggests detecting some sort of endpoint, Han in combination with Sandhu fails to address removing conductive material from the underlying layers without contributing to the thinning of underlying layers. However, in Claims 30, 56, the Applicant teaches removing the conductive and sacrificial layers using a chemical mechanical polishing process so as to inhibit thinning of the dielectric layer during the chemical mechanical polishing process. In addition, since the sacrificial layer is interposed between the shield layer and the conductive layer, CMP removal of the conductive layer and the sacrificial layer down to the shield layer reduces the likelihood that conductive material is left on

the shield layer. Therefore, the Applicant's invention as defined by Claims 30, 56 results in a more consistent removal of excess material without thinning of the shield or dielectric layers as a result of interposing the sacrificial layer.

Moreover, the Sandhu et al. reference is directed towards removing coatings to form insulating spacers between IC devices (See Col. 3, lines 33-37) and is not specifically directed toward removing conductive material deposited on dielectric layers while using sacrificial and shield layers to inhibit thinning of underlying dielectric layers. Therefore, an artisan would not be motivated to combine this reference with the Han reference. Even if Han and Sandhu could be combined, the combination of these references still fails to teach Claims 30, 56 as amended. In addition, the Sandhu et al. reference does not disclose positioning both a sacrificial layer and a shield layer between dielectric layers and the deposited conductive material. Hence, even if both Han and Sandhu were combined, the combination would still fail to teach the concept of positioning a shield layer under a sacrificial layer to inhibit thinning of the underlying dielectric layer during the CMP removal of the conductive material. For these reasons, the Applicant submits that Claims 30, 56 as amended are patentable over the art of record.

Attached hereto is a marked-up version of the changes made to the application by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**; additions are shown as underlined and deletions are shown **[bracketed]**.

SUMMARY

From the foregoing, the Applicant believes that the present application is in condition for allowance, and the Applicant requests the prompt allowance of the same. In light of the above discussion, the Applicant respectfully request reconsideration of the remaining claims which further define patentable subject matter and are allowable due to their dependencies on Claims 30, 56. The undersigned has made a good faith effort to respond to all of the rejections in the case and to place the application in condition for immediate allowance. Nevertheless, if any undeveloped issues remain or if any issues require clarification, the Examiner is respectfully requested to call the undersigned at the number shown below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 12/30/02

By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

30. (Amended) A method of forming a dielectric layer of a first thickness on a semiconductor wafer comprising:

forming the dielectric layer of the first thickness on the wafer;

positioning a shield layer on the dielectric layer;

positioning a sacrificial layer on the shield layer;

depositing conductive material on the sacrificial layer;

removing the conductive material and the sacrificial layer using a chemical mechanical polishing process adapted to remove the conductive material and the sacrificial layer until the shield layer is reached, wherein the shield layer is more resistant to planarization by the chemical mechanical polishing process than the sacrificial layer, and wherein the shield layer inhibits thinning of the dielectric layer during the chemical mechanical polishing process, and wherein interposing the sacrificial layer between the conductive material and the shield layer reduces the amount of conductive material on the shield layer following the chemical mechanical polishing process; and

detecting when the chemical mechanical polishing process has removed the sacrificial layer.

56. (Amended) A method of forming a dielectric layer of a first thickness on a semiconductor wafer comprising:

forming the dielectric layer of the first thickness on the wafer;

positioning a shield layer on the dielectric layer;

positioning a sacrificial layer on the shield layer;

depositing conductive material on the sacrificial layer;

removing the conductive material and the sacrificial layer using a chemical mechanical polishing process adapted to remove the conductive material and the sacrificial layer until the shield layer is reached, wherein the shield layer is more resistant to planarization by the chemical mechanical polishing process than the sacrificial layer, and wherein the shield layer inhibits thinning of the dielectric layer during the chemical mechanical polishing process, and wherein

interposing the sacrificial layer between the conductive material and the shield layer reduces the amount of conductive material on the shield layer following the chemical mechanical polishing process;

selecting an etchant for use with the chemical mechanical polishing process to facilitate removal of the sacrificial layer, and wherein the shield layer is selected to be resistant to the selected etchant; and

detecting when the chemical mechanical polishing process has removed the sacrificial layer.

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